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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,725	05/23/2001	Shirish Gadre	SONY-50P4107	2789

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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER

SORRELL, ERON J

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/864,725

Applicant(s)

GADRE ET AL.

Examiner

Eron J. Sorrell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 and 20-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 and 20-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 3 recites the limitation "said device" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim.

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Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3,6-11,15-18,20, and 23-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Baker et al. (U.S. Patent No. 6,347,344 hereinafter "Baker").

7. Referring to apparatus claims 1,10, and method claim 20, Baker teaches a data and communication apparatus communicatively coupled with a multi-processor shared memory multimedia chip system (see figures 1C and 1D) for providing interprocessor communication while enhancing performance of each processor integral with said multi-processor shared memory multimedia chip system (see lines 23-33 of column 6), said data and communication apparatus comprising:

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a data memory (see item 108 in figure 1a) to retrievably store data (see lines 9-25 of column 7);

an instruction memory (see item 110 in figure 1a) coupled with said data memory to retrievably store instructions (see lines 9-25 of column 7);

an incoming buffer (item 206 in figure 11) coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data (see lines 20-27 of column 37, note the output of the incoming buffer is coupled to the data streamer); and

an outgoing buffer (item 208 in figure 11) coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables said each processor to communicate with other processors disposed within said system (see lines 33-61 and lines 8-16 of column 4, wherein capability of simultaneous transfers is disclosed).

8. Referring to claims 2, 11, and 27 Baker teaches the data and communication apparatus further comprising: multiple registers coupled with said data and communication apparatus (see lines 27-32 of column 12), the registers adapted to provide enhanced

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configurability and control of said data and communication apparatus, the registers further adapted to provide addressable memory storage locations for said retrievably stored data and said retrievable stored instructions, the registers separate from and in addition to the registers within said multi-processor shared memory multimedia chip system (see lines 27-32 of column 12).

9. Referring to apparatus claims 3 and 12, Baker teaches the data and communication apparatus is coupled with said multi-processor shared memory multimedia chip system (see figures 1C and 1D and lines 23-33 of column 6), wherein access to the data and communication apparatus is via an I/O space, said I/O space separate from a memory space of said device, said I/O space pre-existent within said system (see lines 18-29 of column 4).

10. Referring to claims apparatus 6,15, and method claims 23 and 24, Baker teaches the instructions said retrievably stored in said instruction memory are a function of a particular process, said function having certain tendencies relative to said particular process, wherein after said particular process is completed, said function of said particular process is removed, such that a subsequent function of a subsequent process

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is then stored in said instruction memory unit (see paragraph bridging columns 6 and 7).

11. Referring to apparatus claims 7,16, and method claim 28, Baker teaches the incoming buffer is configured as a prefetch mechanism for a particular type of data (see lines 24-37 of column 29), so as to enable acceleration of the rate of said incoming buffer's decoding and parsing of header information relative to said particular data type, such that the processing time of said particular type of data is reduced (see lines 23-33 of column 6).

12. Referring to apparatus claims 8,17, and method claim 25, Baker teaches the outgoing buffer enables said a processor of said multi-processor multimedia chip system to send the communications to other processors disposed within the multi-processor multimedia chip system while independently processing other tasks, such that the processing of said other tasks is not disrupted (see lines 8-16 of column 4).

13. Referring to apparatus claims 9,18, and method claim 26, Baker teaches the outgoing buffer enables said a processor of said multi-processor multimedia chip system to send said

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communications to other processors disposed within said multi-processor multimedia chip system while independently processing other tasks, such that said processing of said other tasks is not disrupted (see lines 61-67 of column 37, note the buffers monitor the amount of data and can generate signals indicating overflow).

14. Referring to claim 29, Baker teaches the data memory is a shared addressable memory (see lines 35-53 of column 40).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 4,13, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker in view of Petrick et al. (U.S. Patent No. 5,892,966 hereinafter "Petrick").

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17. Referring to apparatus claims 4,13, and method claim 21 Baker teaches the apparatuses of claims 1 and 10 and the method of claim 20, (see rejection above), however Baker fails to teach the data said retrievably stored in said data memory is an interrupt service routine (ISR), wherein access to retrieve said interrupt service routine is via said I/O space, such that traffic on said memory space is commensurately reduced, so as to ensure the time required to complete said interrupt service routine.

Petrick teaches, in an analogous system, an ISR stored in data memory and accessed through I/O space (see lines 28-47 of column 13).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the apparatus of Baker with the above teachings of Petrick. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modification in order for the main processor to quickly access interrupts and interrupt values indicating the status of the multimedia coprocessor, while hiding memory latency in multimedia operations (see lines 1-35 of column 5).

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18. Claims 5,14, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker in view of Toy (U.S. Patent No. 4,386,402).

19. Referring to apparatus claims 5,14, and 22, Baker teaches the apparatuses of claims 1 and 10 and the method of claim 20, (see rejection above), however Baker fails to the data retrievably stored in said data memory unit is real-time kernel thread context data, wherein said access to retrieve said real-time kernel thread context data is via said I/O space, such that traffic on said memory space is commensurately reduced, so as to increase speed with which thread context switching is achieved.

Toy teaches, in an analogous context data stored in a data memory and accessed via I/O space (see lines 26-55 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system and method Baker with the above teachings of Toy. One of ordinary skill in the art would have been motivated to make such modification in order to quickly process the interrupt and return to the operations being performed before the interrupt occurred as suggested by Toy (see lines 26-55 of column 4).

Response to Arguments

20. Applicant's arguments with respect to claims 1-18 and 20-29 have been considered but are moot in view of the new ground(s) of rejection.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
February 23, 2006



KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/24/06